# ABSTRACT

Methods and devices are disclosed which provide for memory devices having reduced memory cell square feature sizes. Such square feature sizes can permit large memory devices, on the order of a gigabyte or large, to be fabricated on one chip or die. The methods and devices disclosed, along with variations of them, utilize three dimensions as opposed to other memory devices which are fabricated in only two dimensions. Thus, the methods and devices disclosed, along with variations, contains substantially horizontal and vertical components.